UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,220	09/28/2001	Dong-Yuan Chen	42390P11197	7151

7590 03/28/2006

Blakely, Sokoloff, Taylor & Zafman
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2192	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/967,220	CHEN ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-15,17-25 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-15,17-25 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 30, 2005 has been entered. Claims 1-5, 7-15, 17-25 and 27-30 are pending.

Response to Arguments

2. Applicant's arguments have been fully considered but they are not persuasive.

Applicant contends, with respect to claims 1 and 11, that Levine does not teach or disclose storing traces that are captured by one or more hardware monitors. Specifically, Applicant notes that in Levine, "the address of an instruction being executed is saved in a sampled instruction address register and the effective address of its operand is saved in a sampled data address register," and concludes that "saving the address of an instruction is not equivalent to storing traces because the address of an instruction does not provide information about the actions performed by the instruction" (remarks, page 9, last paragraph).

However, the examiner does not agree. First, there is nothing recited in the claims to limit or specify what information is captured or included in the "traces." At most, Applicant's specification indicates that a "trace" is a "record of the actions carried out by a computer system" (specification, page 3, lines 5-6). Still, although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Nonetheless, storing the effective addresses of instructions and operands, as Levine does, certainly provides a record of the actions carried out by the computer system. Specifically, it provides a record of which instructions and operands were executed. Moreover, Levine expressly discloses that the effective addresses are stored to provide information about long cache misses in the computer system (see, for example, column 11, lines 24-34).

Applicant similarly concludes, with respect to claim 21, that "saving the address of an instruction is not equivalent to storing captured profiles of microarchitecture events because the address of an instruction does not provide any information about profiles of microarchitecture events" (remarks, page 10, middle paragraph).

However, as above, the examiner does not agree with Applicant's characterizations. Levine expressly discloses that the effective addresses are stored to provide information about long cache misses in the computer system (see, for example, column 11, lines 24-34). Cache misses are microarchitecture events (see, for example, column 2, lines 12-14 and column 10, lines 34-36). Moreover, Levine expressly discloses, with reference to FIG. 6, that the "application program is profiled 430 to collect [the] cache miss data" (column 11, lines 25-26, emphasis added). Again, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 7, 10-14, 17, 20-22, 24, 25 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,134,710 to Levine et al. (art of record, "Levine").

With respect to claim 1 (currently amended), Levine discloses a method comprising:

(a) selecting one or more microarchitecture events relating to a microprocessor executing an application process to be monitored by one or more hardware monitors (see, for example, column 2, lines 8-14, which shows selecting events to be recorded by hardware performance monitor counters);

(b) establishing parameters regarding the monitoring of the microarchitecture events by setting one or more monitor control vectors (see, for example, column 2, lines 12-20, which shows setting monitor control registers, i.e. control vectors, to establish monitoring parameters);

(c) storing traces that are captured by the one or more hardware monitors in a first level profile buffer, the first level profile buffer being an architecturally non-visible memory (see, for example, column 10, lines 63-67, which shows storing traces in the sampled instruction and data address registers, i.e. a first level profile buffer that is an architecturally non-visible memory);

(d) transferring the captured traces from the first level profile buffer to a second level profile buffer, the second level profile buffer being an architecturally visible storage (see, for example, column 10, line 67 to column 11, line 3, which shows transferring the traces from the registers to tables in memory, i.e. a second level profile buffer that is an architecturally visible storage);

(e) obtaining the captured traces from the second level profile buffer (see, for example, column 11, lines 34-53, which shows obtaining the traces from the tables in memory);

(f) processing the captured traces (see, for example, column 11, lines 24-34, which shows processing the traces to generate effective address tables);

(g) identifying a region of interest in the application process for optimization based at least in part on the captured traces (see, for example, column 12, lines 1-6, which shows analyzing the effective address tables based on the traces to identify a location or region for optimization); and

(h) optimizing the region of interest in the application process (see, for example, column 13, lines 63 to column 14, line 4, which shows applying the optimizations to the application process).

With respect to claim 2 (original), the rejection of claim 1 is incorporated, and Levine further discloses the limitation wherein setting each monitor control vector comprises setting one or more fields of the monitor control vector to control the monitoring of the microarchitecture event (see, for example, column 2, lines 8-20, which shows setting fields in the control registers to control the event counting or monitoring).

With respect to claim 3 (original), the rejection of claim 2 is incorporated, and Levine further discloses the limitation wherein setting the one or more fields of each monitor control vector includes setting a control field to establish the type of microarchitecture event that is monitored by a hardware monitor (see, for example, column 8, lines 44-52, which shows setting control fields to select the types of events to be monitored).

With respect to claim 4 (original), the rejection of claim 2 is incorporated, and Levine further discloses the limitation wherein setting the one or more fields of each monitor control vector includes setting a trigger field to control when a microarchitecture event is monitored (see, for example, column 8, lines 23-24 and 35-39, which show setting trigger fields to control when events are counted or monitored).

With respect to claim 7 (currently amended), the rejection of claim 1 is incorporated, and Levine further discloses the limitation wherein obtaining the captured traces for a microarchitecture event from the second level profile buffer occurs when a memory buffer in the second level profile buffer that is assigned for the monitored microarchitecture event is fully allocated (see, for example, column 11, lines 42-53, which shows that the buffer is of a predetermined size and is used in a round-robin fashion, and is therefore fully allocated when the traces are obtained before being overwritten).

With respect to claim 10 (original), the rejection of claim 1 is incorporated, and Levine further discloses the limitation wherein the microarchitecture event monitored is an instruction cache miss event (see, for example, column 10, lines 2-8, which shows instruction cache miss

events, and column 10, lines 15-19 and 34-36, which show counting or monitoring such cache misses).

With respect to claim 11 (currently amended), see the rejection of claim 1 above. The operations recited in claim 11 are analogous to the method steps of claim 1. Note that Levine further discloses a machine-readable medium having stored thereon data representing instructions that, when executed by a processor, cause the processor to perform the recited operations (see, for example, column 1, line 65 to column 2, line 1, and column 2, lines 28-44).

With respect to claim 12 (original), the rejection of claim 11 is incorporated, and the operations recited in the claim are analogous to the method steps of claim 2 (see the rejection of claim 2 above).

With respect to claim 13 (original), the rejection of claim 12 is incorporated, and the operations recited in the claim are analogous to the method steps of claim 3 (see the rejection of claim 3 above).

With respect to claim 14 (original), the rejection of claim 12 is incorporated, and the operations recited in the claim are analogous to the method steps of claim 4 (see the rejection of claim 4 above).

With respect to claim 17 (currently amended), the rejection of claim 11 is incorporated, and the operations recited in the claim are analogous to the method steps of claim 7 (see the rejection of claim 7 above).

With respect to claim 20 (original), the rejection of claim 11 is incorporated, and the operations recited in the claim are analogous to the method steps of claim 10 (see the rejection of claim 10 above).

With respect to claim 21 (currently amended), Levine discloses a hardware assisted dynamic optimizer (see, for example, the abstract and FIG. 2), comprising:

(a) an interface to a microprocessor through which the hardware assisted dynamic optimizer establishes parameters regarding the monitoring of one or more microarchitecture events occurring during the execution of an application by the microprocessor (see, for example, column 2, lines 8-20, which shows setting addressable monitor control registers to select events to be recorded and establish monitoring parameters);

(b) one or more handler routines, each handler routine including instructions to process profiles of a monitored microarchitecture event that are captured by the microprocessor (see, for example, column 10, line 67 to column 11, line 5, which shows a handler routine for processing captured profile data, and column 11, lines 24-34, which shows processing the data to generate effective address tables);

(c) a first level profile buffer to initially store captured profiles, the first level profile buffer being architecturally non-visible (see, for example, column 10, lines 63-67, which shows initially storing profile data in the sampled instruction and data address registers, i.e. a first level profile buffer that is architecturally non-visible);

(d) a second level profile buffer to receive captured profiles from the first level profile buffer, the second level profile buffer being architecturally visible (see, for example, column 10,

line 67 to column 11, line 3, which shows receiving the profile data from the registers in tables in memory, i.e. a second level profile buffer that is architecturally visible); and

(e) one or more optimizers, each optimizer including instructions for optimizing a section of the application, the section of the application being chosen by the hardware assisted dynamic optimizer at least in part based on the captured profiles of a monitored microarchitecture event (see, for example, column 12, lines 1-6, which shows analyzing the effective address tables based on the profile data to identify a location or region for optimization, and column 13, line 63 to column 14, line 4, which shows applying the optimizations to the application).

With respect to claim 22 (original), the rejection of claim 21 is incorporated, and Levine further discloses the limitation wherein each monitor control vector includes a plurality of fields to control the monitoring of the microarchitecture event, the plurality of fields being set by the hardware assisted dynamic optimizer (see, for example, column 2, lines 8-20, which shows setting fields in the control registers to control the event counting or monitoring).

With respect to claim 24 (original), the rejection of claim 21 is incorporated, and Levine further discloses the limitation wherein optimizing a section of the application includes increasing the speed of processing of the section of the application (see, for example, column 1, lines 19-23, which shows that delays in executing an application may be caused by long table walks or long cache misses, and see, for example, column 1, lines 58-62, which shows that the optimizations minimize the effects of such table walks and cache misses, i.e. increase the speed of processing the application).

With respect to claim 25 (previously presented), the rejection of claim 21 is incorporated, and Levine further discloses the limitation wherein the hardware assisted dynamic optimizer obtains the captured profiles of the one or more microarchitecture events from the second level profile buffer (see, for example, column 11, lines 34-53, which shows obtaining the profile data from the tables in memory).

With respect to claim 27 (previously presented), the rejection of claim 21 is incorporated, and Levine further discloses the limitation wherein the hardware assisted dynamic optimizer sets conditions for transferring captured profiles from the first level profile buffer to the second level profile buffer (see, for example, column 10, line 67 to column 11, line 3, which shows transferring the profile data from the registers to the tables in memory when an interrupt is serviced, and column 8, lines 24-35, which shows setting conditions for the interrupt).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 15 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levine, as applied to claims 2, 12 and 22 above, respectively.

With respect to claim 5 (currently amended), the rejection of claim 2 is incorporated. Levine discloses setting an interrupt field to cause a handler routine to process the traces when an

event occurs (see, for example, column 8, lines 24-35, which shows the interrupt field in the control register, and column 10, line 67 to column 11, line 5, which shows the handler routine).

Levine does not expressly disclose the limitation wherein setting the one or more fields of each monitor control vector includes storing a pointer in a handler field, the pointer identifying a handler routine to process the captured traces corresponding to the monitor control vector.

However, a pointer is inherently used in the Levine system to identify the handler routine. The address of the routine must be known in order to invoke the routine and process the captured traces. It is also well known in the art that a pointer may be stored, for example, in a field of a control vector or register.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the pointer to the handler routine of Levine in a field of the control registers taught by Levine, for the purpose of identifying the address of the routine.

With respect to claim 15 (currently amended), the rejection of claim 12 is incorporated, and the operations recited in the claim are analogous to the method steps of claim 5 (see the rejection of claim 5 above).

With respect to claim 23 (original), the rejection of claim 22 is incorporated, and Levine further discloses the limitation wherein the plurality of fields includes:

(a) a control field to establish the type of microarchitecture event that is monitored (see, for example, column 8, lines 44-52, which shows setting control fields to select the types of events to be monitored), and

(b) a trigger field to control when the microarchitecture event is monitored (see, for example, column 8, lines 23-24 and 35-39, which show setting trigger fields to control when events are counted or monitored).

Although Levine discloses setting an interrupt field to cause a handler routine to process the profile data when an event occurs (see, for example, column 8, lines 24-35, which shows the interrupt field in the control register, and column 10, line 67 to column 11, line 5, which shows the handler routine), Levine does not expressly disclose the limitation wherein the plurality of fields includes:

(c) a handler field to store a pointer to the handler routine for the microarchitecture event.

However, a pointer is inherently used in the Levine system to identify the handler routine. The address of the routine must be known in order to invoke the routine and process the captured profile data. It is also well known in the art that a pointer may be stored, for example, in a field of a control vector or register.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the pointer to the handler routine of Levine in a field of the control registers taught by Levine, for the purpose of identifying the address of the routine.

7. Claims 8, 9, 18, 19 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levine, as applied to claims 7, 17 and 27 above, respectively, in view of U.S. Patent No. 6,622,300 to Krishnaswamy et al. (art of record, "Krishnaswamy").

With respect to claim 8 (currently amended), the rejection of claim 7 is incorporated, and Levine further discloses setting one or more conditions for transferring captured traces from the

first level profile buffer to the second level profile buffer (see, for example, column 10, line 67 to column 11, line 3, which shows transferring the traces from the registers to the tables in memory when an interrupt is serviced, and column 8, lines 24-35, which shows setting conditions for the interrupt).

Levine does not expressly disclose setting one or more conditions for obtaining captured traces when the memory buffer in the second level profile buffer is not fully allocated.

However, Krishnaswamy discloses storing profile data in a buffer and reading the data from the buffer by setting an interrupt condition after a certain number of events, i.e. obtaining the data when the buffer is not fully allocated, so as to sample the profile data nonintrusively without significantly degrading performance (see, for example, column 6, lines 21-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to set a condition for obtaining the traces of Levine when the memory buffer is not fully allocated, so as to sample the traces nonintrusively without significantly degrading performance, such as taught by Krishnaswamy.

With respect to claim 9 (currently amended), the rejection of claim 8 is incorporated, and Krishnaswamy further discloses receiving an interrupt or special event handler if the memory buffer that is assigned for the microarchitecture event is fully allocated or if a condition for obtaining captured traces when the memory buffer in the profile buffer is not fully allocated is met (see, for example, column 6, lines 21-45, which shows receiving an interrupt for obtaining the profile data from the buffer when the event-counting condition is met).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an interrupt for obtaining the traces of Levine from the memory buffer, so as to

sample the traces nonintrusively without significantly degrading performance, such as taught by Krishnaswamy.

With respect to claim 18 (currently amended), the rejection of claim 17 is incorporated, and the operations recited in the claim are analogous to the method steps of claim 8 (see the rejection of claim 8 above).

With respect to claim 19 (currently amended), the rejection of claim 18 is incorporated, and the operations recited in the claim are analogous to the method steps of claim 9 (see the rejection of claim 9 above).

With respect to claim 28 (previously presented), the rejection of claim 27 is incorporated. Levine does not expressly disclose the limitation wherein the hardware assisted dynamic optimizer sets one or more conditions for obtaining captured profiles from the second level profile buffer.

However, Krishnaswamy discloses storing profile data in a buffer and reading the data from the buffer by setting an interrupt condition after a certain number of events, so as to sample the profile data nonintrusively without significantly degrading performance (see, for example, column 6, lines 21-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to set a condition for obtaining the profile data of Levine, so as to sample the profile data nonintrusively without significantly degrading performance, such as taught by Krishnaswamy.

With respect to claim 29 (previously presented), the rejection of claim 28 is incorporated, and Levine further discloses the limitation wherein a memory buffer in the second level profile buffer is assigned to a microarchitecture event, and wherein the hardware assisted dynamic optimizer accesses the profiles of the microarchitecture event when the memory buffer assigned to the microarchitecture event is fully allocated or when a condition for obtaining captured profiles is met (see, for example, column 11, lines 42-53, which shows that the buffer is of a predetermined size and is used in a round-robin fashion, and is therefore fully allocated when the profile data is obtained before being overwritten).

With respect to claim 30 (original), the rejection of claim 29 is incorporated, and Krishnaswamy further discloses the limitation wherein the hardware assisted dynamic optimizer accesses the profiles of a microarchitecture event upon receiving an interrupt or special event handler (see, for example, column 6, lines 21-45, which shows obtaining the profile data upon receiving an interrupt).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an interrupt for obtaining the profile data of Levine, so as to sample the profile data nonintrusively without significantly degrading performance, such as taught by Krishnaswamy.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2192

mjy

TUAN DAM
SUPERVISORY PATENT EXAMINER